REMARKS

This amendment accompanies a request for continued examination (RCE).

Claims 1-3 and 6-14 are pending for further examination. Claims 1 and 8 are currently amended. Claims 13 and 14 are new.

Claims 1-3 and 6-13 were rejected under 35 U.S.C. § 102(b) as anticipated by Takeda (U.S. Patent No. 6,014,318). As discussed below, applicants disagree and respectfully request reconsideration of the pending claims.

Currently amended independent claims 1 and 8 recite, in part, a semiconductor device that includes a mounting substrate of a "single layer resin material" having first and second main surfaces. A step portion in the periphery of the first main surface of the mounting substrate extends to "about the middle of the substrate in a thickness direction." Support for these features may be found in the specification on pg. 5, lines 23-24 which disclose that the mounting substrate 11 may be composed of, for example, a glass epoxy material and on pg. 6, lines 2-6 which disclose that the depth of step portion 15 can be about half the thickness of the mounting substrate. The example of FIG. 1B also shows only a single material forming the mounting substrate 11. In some implementations, these features may reduce the number of materials required for fabrication and improve adhesion between the mounting substrate and a sealing resin. The Takeda patent neither discloses nor suggests the claimed mounting substrate with a step portion.

The Takeda patent discloses a package structure that includes a wiring substrate 101 (*see* FIG. 4). Chips 121, 122 are mounted on the substrate 101. Conductive elements are exposed at upper and lower surfaces of the substrate 101. Solder bumps 112 are exposed at the lower surface of the package structure. Portions of the upper and side surfaces of the substrate 101 are covered with sealing resin 103. A solder resist 105 covers the back of the substrate 101 except for the regions where the solder bumps 112 are formed.

The Office action alleges (pg. 3) that the region on the surface of the wiring substrate 101, where sealing resin 103 is formed, corresponds to the "first main surface" of a mounting substrate and that the region where sealing resin 103 is not formed on solder resist 105

corresponds to the "second main surface" of a mounting substrate as recited in present claims 1 and 8. The Office action further alleges that the claimed "step portion" is formed at the periphery of the first main surface and that solder bumps 112 of the Takeda patent correspond to the claimed "second conductive pattern" formed on the second main surface of the mounting substrate. Applicants respectfully disagree.

The solder resist 105 and wiring substrate 101 of the Takeda patent do not correspond to the claimed mounting substrate. It is well known by those of ordinary skill in the art that solder resist is used to prevent solder bridges from forming during soldering but is not used, by itself or in part, as a substrate for mounting devices. Furthermore, FIG. 1 clearly shows that the solder resist 105 and wiring substrate 101 do not correspond to a "*single layer* of resin material" as recited in present claims 1 and 8. Rather, substrate 101 and resist 105 are shown as two *separate* layers.

However, even if the solder resist 105 and substrate 101 correspond to the claimed mounting substrate, which is incorrect, the solder bumps 112 of the Takeda patent are not "formed on the second main surface of the mounting substrate" as further recited in present claims 1 and 8. Instead, the solder bumps are formed on the surface of material P1 (*see* pg. 4, Office action), which the Office action asserts corresponds to the claimed plating line, that extends through the wiring substrate 101. Material P1 provides a connection between the solder bumps and metal wires connecting the chips but is not, by itself or in part, a mounting substrate. Nor does the material P1 correspond to both the claimed plating line and mounting substrate.

At least for the foregoing reasons, independent claims 1 and 8 should be allowed.

Claims 2-3, 6-7, 13 and 9-12, 14 respectively depend from claims 1 and 8 and should be allowed for at least the same reasons.

Furthermore, the dependent claims recite features that make the claims independently patentable. For example, claims 13 and 14 recite that a first conductive pattern extends laterally to the edge of the of the first main surface. In contrast, the conductive pattern C1 of the Takeda patent (*see* pg. 4, Office action), which the Office action asserts corresponds to the claimed first conductive pattern, ends short of the edge of the top surface of substrate 101.

For this additional reason, claims 13 and 14 should be allowed.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

The RCE fee in the amount of $790 is being paid concurrently herewith on the Electronic Filing System (EFS) by way of Deposit Account authorization. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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